In the Claims:

1-24. (canceled)

25. (amended) A method of ~~communicating with~~ reading words of data from a device coupled to ~~a target interface circuit associated with~~ a register, which is in series with a serial data output, ~~bus coupled to a plurality of interface circuits,~~ comprising ~~the steps of~~:

A. loading a controller with control data to provide read data control signals to the register and the device;

B. transferring a word of data in parallel from the device into ~~a~~ the register ~~associated with the target interface circuit~~ in response to the control signals;

C. shifting data from the register ~~onto~~ in series to the serial data output ~~bus~~ in response to the control signals; and

D. ~~transferring~~ repeating steps B. and C. for additional words of data ~~from the device into the register~~ after the last data bit of the previous word of data is shifted out of the register without loading the controller with additional control data.

26. (amended) The method of claim 25 ~~wherein said step of~~ in which shifting data from the register ~~comprises the step of~~ includes shifting data ~~sequentially through ones of said interface circuits~~ into another register.

27. (amended) The method of claim ~~26 and further comprising the step of~~ 25 including counting the number of data bits ~~transferred~~ shifted from the register.

28. (amended) The method of claim ~~26 and further comprising the step of~~ 25 including generating a control signal indicating that ~~the data stored in the register has been transferred~~ shifting data to the ~~bus~~ output is complete.

29. (amended) The method of claim 25 ~~and further comprising the steps of: shifting data onto the bus and sequentially through each interface circuit preceding the target interface circuit; generating a control signal indicative of said data shifted onto the bus reaching said target interface circuit; and transferring data from a register associated with said target interface circuit to said device responsive to said control signal~~ including ceasing the repeating steps B. and C. after a certain number of data words have been shifted from the register to the output.

30-36. (canceled)

37. (new) A process of reading words of data from a memory comprising:

A. loading a control register with control data to select a memory access controller;

B. transferring a word of data in parallel from the memory into a data register in response to first control signals in a first state;

C. shifting data from the data register in series in response to first control signals in a second state;

D. transferring a word of data in parallel from the memory into the data register after the last data bit of the previous word of data is shifted out of the data register in response to memory access control signals from the memory access controller while maintaining the first control signals in the second state; and

E. shifting data from the data register in series in response to memory access control signals from the memory access controller while maintaining the first control signals in the second state.

38. (new) The process of claim 37 including repeating steps D. and E. for additional words of data.

39. (new) The process of claim 37 including stopping the reading of words from the memory by changing the first control signals to a third state.

40. (new) The process of claim 37 including counting the number of data bits shifted from the data register.

41. (new) The process of claim 37 including producing an end signal when the last data bit of a word is shifted out of the data register.

42. (new) The process of claim 37 in which the transferring and shifting steps respectively transfer and shift eight bit words of data.